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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/902,170	07/11/2001	Masahiko Ando	H6810.0011/P011	8805

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DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 06/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/902,170	ANDO ET AL.
	Examiner	**Art Unit**
	Khiem D Nguyen	2823

-- Th MAILING DATE of this communication appears on th cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _07 April 2003_ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-98_ is/are pending in the application.

4a) Of the above claim(s) _35-49 and 84-98_ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-34 and 50-83_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _11 July 2001_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on _07 April 2003_ is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on April 7, 2003 have been approved by the examiner. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

Response to Amendment

Response to Arguments

Applicant's arguments with respect to claims 1-34 and 50-83 have been considered but are moot in view of the new ground(s) of rejection.

New Grounds of Rejection

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art of this application (AAPA) in view of Ting (U.S. Patent 6,214,705) and Washizuka et al. (IDW 1997 pp. 207-210).

AAPA discloses a method of fabricating a thin film transistor comprising the steps of (See Discussion of the Related Art on page 1-2 of this application and FIG. 6(a)-(d)):

providing a gate (FIG. 6(d), 62) over a substrate (FIG. 6(d), 61);

providing a gate insulating layer (FIG. 6(d), 63) over the gate and substrate;

providing an amorphous silicon layer (FIG. 6(d), 64) having a high resistance over the gate insulating layer;

providing an impurity over the amorphous silicon layer (FIGS. 6(a)-(b));

forming a drain electrode (FIG. 6(d), 66) and source electrode (FIG. 6(d), 67) separated by a channel region over a contact portion with the amorphous silicon layer; and,

removing the impurity from the channel region (FIG. 6 (c)) to form a contact layer (FIG. 6(d), 65) within the amorphous silicon layer wherein the contact layer has a second resistance lower than the first resistance (page 2, lines 3-10).

AAPA fails to explicitly disclose diffusing the impurity into the contact portion by an annealing process wherein the annealing is conducted at a temperature of about 300°C-320°C for about 10-15 minutes and wherein the impurity is phosphorus as recited in present claims 5-7, 17-19 and 28-30.

Ting discloses diffusing the impurity into the amorphous silicon layer by an annealing process wherein the impurity is phosphorus and wherein the annealing is conducted at a temperature of about 500°C-600°C (col. 2, line 47 to col. 3, line 10). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of AAPA and Ting to enable the process of diffusing the impurity into the contact region of AAPA to be performed and furthermore to lower the resistance of the gate electrode (col. 3, lines 4-6).

Ting fails to explicitly disclose the annealing temperature and time duration as recited in present claims 6, 18, and 29. However, the annealing temperature and time duration are result-effective variables and there is no evidence indicating that the annealing temperature and time duration are critical and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

AAPA fails to explicitly disclose the thickness of the amorphous silicon film, the concentration of the impurity, and the exposure time as recited in present claims 2, 4, 8, 14, 16, 20, 25, 27, and 29. However, it has been held that it is not inventive to discover the optimum or workable thickness, concentration of the impurity, and the exposure time of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

AAPA fails to explicitly disclose removing the impurity from the channel region is performed by exposure to hydrogen plasma as recited in present claims 3, 15, and 26. However, the process of removing the impurity by expose to hydrogen plasma is well-known to one of ordinary skill in the art of making semiconductor devices.

AAPA fails to explicitly disclose that the diffusing step is performed simultaneously with an annealing step for a capping layer provided over the electrodes and the channel region as recited in present claims 9, 21, and 32. However, selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results. In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946).

AAPA fails to explicitly disclose wherein the amorphous silicon layer is etched utilizing a common photoresist to form the electrodes as recited in present claims 11, 13 and 24.

Washizuka discloses etching the amorphous silicon layer utilizing a common photoresist to form the electrodes (page 208 and FIG. 3). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of AAPA and Washizuka to enable the electrodes of AAPA to be formed and furthermore to achieve high image quality of TFT-LCDs (page 207).

2. Claims 50-83 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art of this application (AAPA) in view of Ting (U.S. Patent 6,214,705) and Washizuka et al. (IDW 1997 pp. 207-210).

AAPA discloses a method of fabricating a liquid crystal display (LCD) comprising the steps of (See Discussion of the Related Art on page 1-2 of this application and FIG. 6(a)-(d)):

providing a plurality of thin film transistors arranged on a LCD substrate in a matrix form, each of the thin film transistors fabricated by the steps of:

providing a gate (FIG. 6(d), 62) over a substrate (FIG. 6(d), 61);

providing a gate insulating layer (FIG. 6(d), 63) over the gate and substrate;

providing an amorphous silicon layer (FIG. 6(d), 64) having a high resistance over the gate insulating layer;

providing an impurity (FIGS. 6(a)-(b)) over the amorphous silicon layer;

forming a drain electrode (FIG. 6(d), 66) and source electrode (FIG. 6(d), 67) separated by a channel region over a contact portion with the amorphous silicon; and,

removing the impurity from the channel region (FIG. 6(c)) to form a contact layer (FIG. 6(d), 65) within the amorphous silicon layer, wherein the contact layer has a second resistance lower than the first resistance (page 2, lines 3-10).

AAPA fails to explicitly disclose diffusing the impurity into the contact portion by an annealing process wherein the annealing is conducted at a temperature of about 300°C-320°C for about 10-15 minutes and wherein the impurity is phosphorus as recited in present claims 54-56, 66-68, and 77-79.

Ting discloses diffusing the impurity into the amorphous silicon layer by an annealing process wherein the impurity is phosphorus and wherein the annealing is conducted at a temperature of about 500°C-600°C (col. 2, line 47 to col. 3, line 10). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of AAPA and Ting to enable the process of diffusing the impurity into the contact region of AAPA to be performed and furthermore to lower the resistance of the gate electrode (col. 3, lines 4-6).

Ting fails to explicitly disclose the annealing temperature and time duration as recited in present claims 55, 67, and 78. However, the annealing temperature and time duration are result-effective variables and there is no evidence indicating that the annealing temperature and time duration are critical and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

AAPA fails explicitly disclose the thickness of the amorphous silicon film, the concentration of the impurity, and the exposure time as recited in present claims 51, 53, 57, 63, 65, 69, 74, 76, and 80. However, it has been held that it is not inventive to discover the optimum or workable thickness, concentration of the impurity, and the exposure time of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

AAPA fails to explicitly disclose removing the impurity from the channel region is performed by exposure to hydrogen plasma as recited in present claims 52, 64, and 75. However, the process of removing the impurity by expose to hydrogen plasma is well-known to one of ordinary skill in the art of making semiconductor devices.

AAPA fails to explicitly teach that the diffusing step is performed simultaneously with an annealing step for a capping layer provided over the electrodes and the channel region as recited in present claims 58, 70, and 81. However, selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results. In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946).

AAPA fails to explicitly disclose wherein the amorphous silicon layer is etched utilizing a common photoresist to form the electrodes as recited in present claims 60, 62, and 73.

Washizuka discloses etching the amorphous silicon layer utilizing a common photoresist to form the electrodes (page 208 and FIG. 3). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching

of AAPA and Washizuka to enable the electrodes of AAPA to be formed and furthermore to achieve high image quality of TFT-LCDs (page 207).

Response to Amendment

Response to Arguments

Applicant's arguments with respect to claims 1-34 and 50-83 have been considered but are moot in view of the new ground(s) of rejection.

In response to applicant's argument that the applicant's prior art (AAPA) does not teach providing an impurity over the amorphous silicon layer, AAPA discloses providing an impurity (FIGS. 6(a)-(b)) over the amorphous silicon layer (FIG. 6(d), 64) and removing the impurity from the channel region (FIG. 6(c)) to form a contact layer (FIG. 6(d), 65) within the amorphous silicon layer, wherein the contact layer has a second resistance lower than the first resistance (page 2, lines 3-10).

In response to applicant's argument that Ting does not teach or suggest diffusing impurity ions into the amorphous silicon layer, Ting discloses diffusing the impurity into the amorphous silicon layer by an annealing process wherein the impurity is phosphorus and wherein the annealing is conducted at a temperature of about 500°C-600°C (col. 2, line 47 to col. 3, line 10). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of AAPA and Ting to enable the process of diffusing the impurity into the contact region of AAPA to be performed and furthermore to lower the resistance of the gate electrode (col. 3, lines 4-6).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (703) 306-0210. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-9179 for regular communications and (703) 746-9179 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
June 4, 2003

Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800